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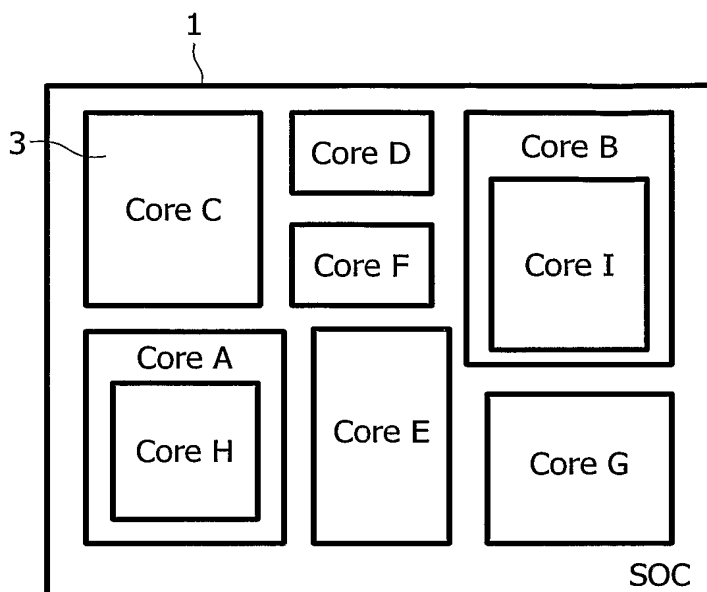
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(54) Title: TEST CIRCUIT AND METHOD FOR HIERARCHICAL CORE



(57) Abstract: A wrapper architecture has a parent core A and a child core B. The parent core A comprises scan chains (70), wrapper input cells (71), wrapper output cells (74) and a parent TAM, PTAM [0:2]. Likewise, the child core comprises scan chains (76), wrapper input cells (75) and wrapper output cells (72), and is connected to a child TAM, CTAM [0:2]. Each wrapper input cell (75) and each wrapper output cell (72) of the child core is adapted to be connected to the parent TAM, PTAM, in addition to being connected to the child TAM, CTAM, thereby enabling the child core to be placed in the In-test and Ex-test modes at the same time, and allowing the parent and child cores to be tested in parallel.



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